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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,052	03/22/2004	Uway Tseng	P910146CIP	1518

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EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,052	TSENG ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The finality of the office action mailed 8/4/05 has been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Hurley, US 2003/0013253.

Hurley shows the invention as claimed including a method for forming a memory device, comprising: providing a stacked structure on a substrate 10, the stacked structure comprising a first dielectric 21, a floating gate 22, a second dielectric 33, and a control gate 34; forming a liner dielectric layer 62, which extends in a direction transverse to a bit line direction and substantially parallel to the control gate, on sidewalls of the stacked structure; and forming a barrier layer 63 on at least part of the liner dielectric layer (see figs. 6-9 and paragraphs 0021-0035).

With respect to claim 2, the providing of the stacked structure comprises: forming a first dielectric layer on the substrate; forming a floating gate on the first dielectric layer; forming a second dielectric layer on the floating gate; and forming a control gate on the second dielectric layer.

Regarding claim 3, the forming of a barrier layer comprises forming a silicon nitride layer.

With respect to claims 15-16, note that the liner dielectric and the barrier layer 44 are formed to extend over some source/drain regions and not to extend over other source/drain regions.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-7, 10, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller et al., U.S. Patent 5,985,719 in view of Hurley, US 2003/0013253.

Keller et al. shows the invention as claimed including a method for forming a memory device, comprising: providing a stacked structure on a substrate 32, the stacked structure comprising a first dielectric 36, a floating gate 37, a second dielectric 38, and a control gate 39; forming a liner dielectric layer 42 that extends in a direction substantially parallel to the control gate on sidewalls of the stacked structure; and forming a barrier layer 44 on at least part of the liner dielectric layer (see figs. 3-7 and col. 4-line 35 to col. 5-line 34).

Keller et al. does not expressly disclose the liner direction extending in a direction transverse to a bit line.

Hurley discloses forming source and drain bitlines 93 extending in a direction transverse to a floating gate and control gate (see figs. 7-9 and col. 5-line 66 to col. 8-line 12). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Keller et al. so as to form the liner transverse to the bitline because Hurley shows that it is conventional memory architecture to have the floating and control gate stack transverse to the bitline.

Concerning claim 2, note that in Keller et al. the providing of a stacked structure on a substrate 32 comprises: forming a first dielectric layer 36 on the substrate 32; forming a floating gate 37 on the first dielectric layer 36; forming a second dielectric layer 37 on the floating gate 36; and forming a control gate 39 on the second dielectric layer.

W ith respect to claim 3, note that in Keller et al. the barrier layer is a silicon nitride layer (see col. 4-lines 65-66).

Regarding claim 5, note that the liner dielectric 42 in Keller et al. is formed by performing thermal oxidation (see col. 4-lines 50-53).

Concerning claim 6, note that the barrier layer of silicon nitride in Keller et al. can be formed by chemical vapor deposition (see col. 4-lines 62-63).

With respect to claims 15-16, note that the liner dielectric 42 and the barrier layer 44 in Keller et al. are formed to extend over some source/drain regions and not to extend over other source/drain regions (see fig. 7).

Furthermore, Keller et al. and Hurley are applied as above but fail to expressly disclose wherein the silicon nitride layer is either greater than ten angstroms or greater than thirty angstroms. However, Keller et al. discloses the silicon nitride layer to be in a range from 50 to 200 angstroms (see col. 4-line 67) and therefore a prima facie case of obviousness exists because In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keller et al., U.S. Patent 5,985,719 in view of Hurley, US 2003/0013253 as applied to claims 1-3, 5-7, 10 and 15-16 above, and further in view of Kokubu, U.S. Patent 6,200,858.

Keller et al. and Hurley are applied as above but fails to expressly disclose an oxide spacer on the nitride barrier layer.

Kokubu discloses forming an oxide spacer 9 on the nitride barrier layer 8 (see fig. 1 and col. 2-line 65 to col. 3-line 58). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Keller et al. modified by Hurley so as to form an oxide spacer over the nitride barrier layer as suggested by Kokubu because in such a way leakage of carriers through the sidewalls of the memory device can be suppressed.

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller et al., U.S. Patent 5,985,719 in view of Hurley, US 2003/0013253 as applied to claims 1-3, 5-7, 10 and 15-16 above, and further in view of Tay et al., US 2002/0009900.

Keller et al. and Hurley show the invention as explained above but fail to expressly disclose wherein the forming of the silicon nitride layer comprises performing nitridation using rapid thermal processing in the presence of diatomic nitrogen or nitrous oxide.

Tay et al. discloses heating an oxide film in a RTP chamber in the presence of a nitrogen containing gas such as diatomic nitrogen or nitrous oxide so that a nitrogen containing layer forms on the surface (see paragraphs 0034-0037). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Keller et al. and Hurley to form the nitride barrier layer as suggested by Tay et al. because this is shown to be a suitable method in which to form a nitride layer on an oxide layer.

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller et al., U.S. Patent 5,985,719 in view of Hurley, US 2003/0013253 and further in view of Tay et al as applied to claims 8-9 above, and further in view of Ma et al., U.S. Patent 6,207,586.

Keller et al., Hurley, and Tay et al. are applied as above but fail to expressly disclose forming the silicon nitride layer by subjecting the liner dielectric layer to nitrogen plasma.

Ma et al. discloses exposing an oxide layer 14 with a plasma containing diatomic nitrogen atmosphere to form a nitride layer 16 (see col. 6-line 16 to col. 7-line 35). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Keller et al. modified by Hurley et al. and Tay et al. so as to form the nitrogen layer as suggested by Ma et al. because this is shown to be a suitable method to create a nitride layer from an oxide layer.

Regarding the t hickness of the nitride layer, Keller et al. discloses the silicon nitride layer to be in a range from 50 to 200 angstroms (see col. 4-line 67) and therefore a prima facie case of obviousness exists because In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller et al., U.S. Patent 5,985,719 in view of Hurley, US 2003/0013253 as applied to claims 1-3, 5-7, 10 and 15-16 above, and further in view of Gill, U.S. Patent 5,420,060.

Keller et al. and Hurley are applied as above but fails to expressly disclose the second dielectric comprising a lower layer of insulator material, a middle layer of charge trapping material, and an upper layer of insulator material.

Gill discloses forming the second dielectric layer 11 in the claimed manner by forming the upper and lower layers of oxide material and the middle layer of nitride material (see col. 5-lines 31-33). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Keller et al. modified by Hurley so as to form the oxide-nitride-oxide structure between the floating and control gates of Keller et al. because Gill shows such a layer is a suitable material to be used between floating and control gates in a memory structure.

Response to Arguments

Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard A. Booth
Primary Examiner
Art Unit 2812

February 21, 2006